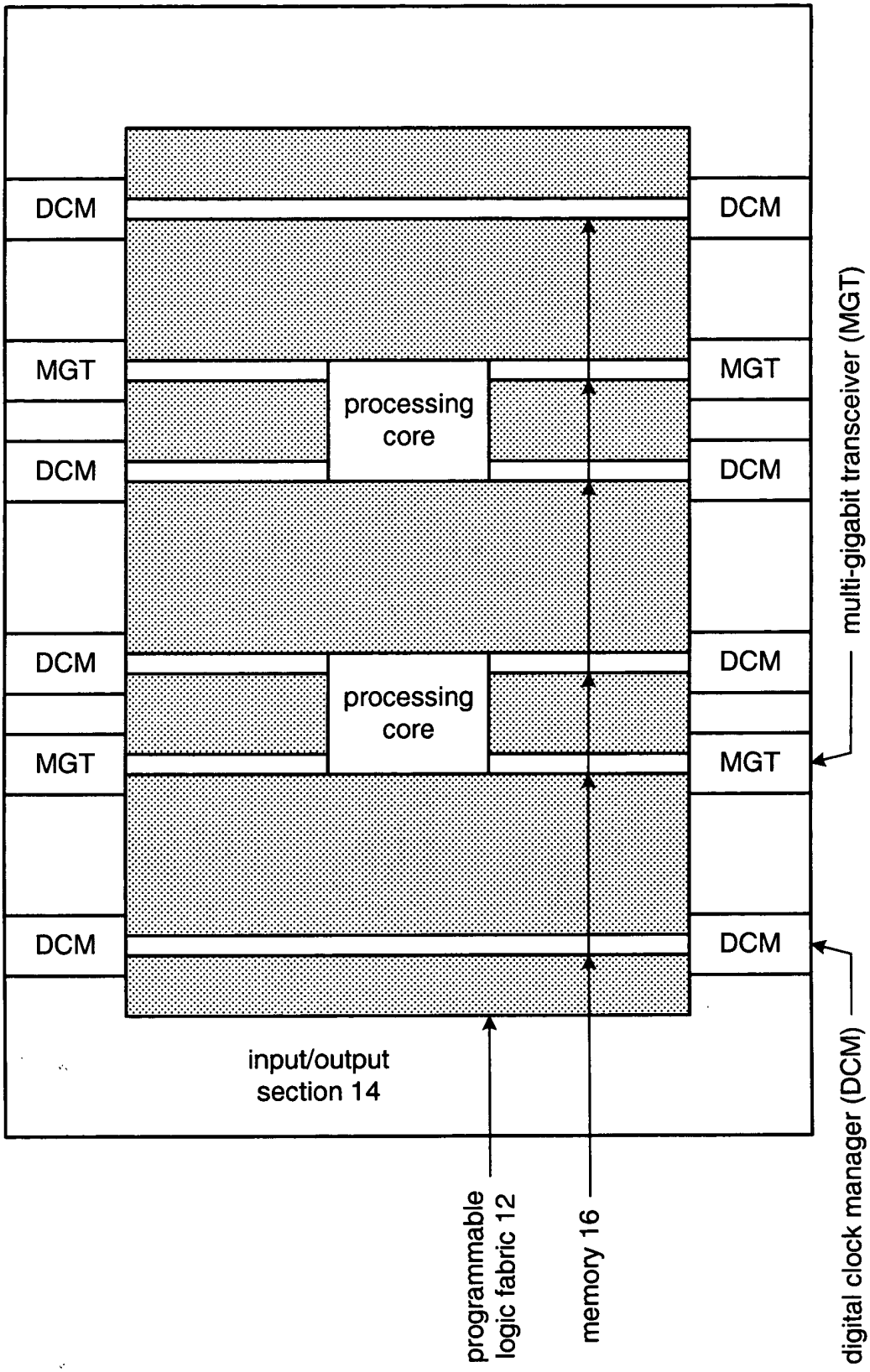

FIG. 1
programmable logic device 10

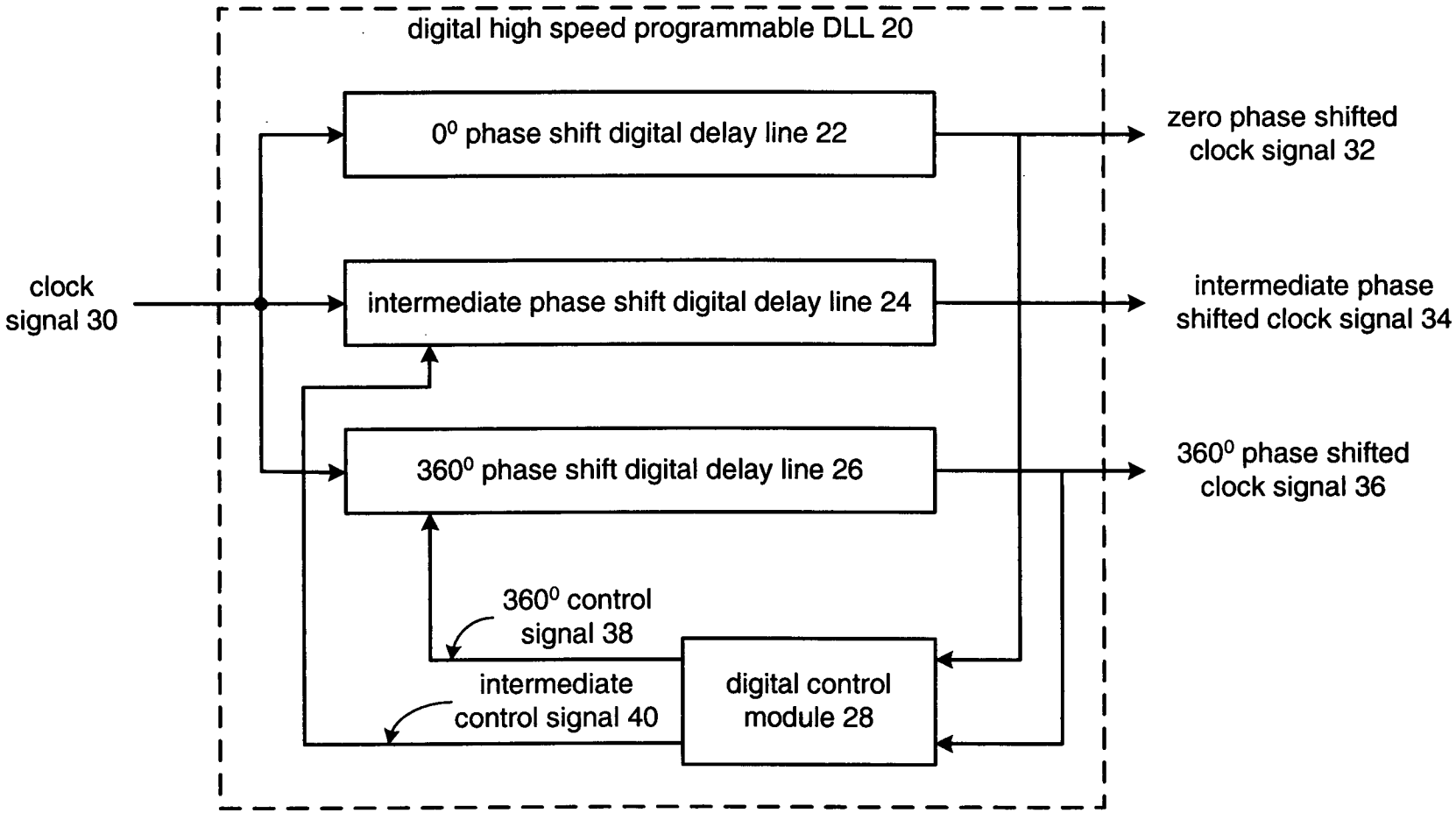

FIG. 2

digital clock manager

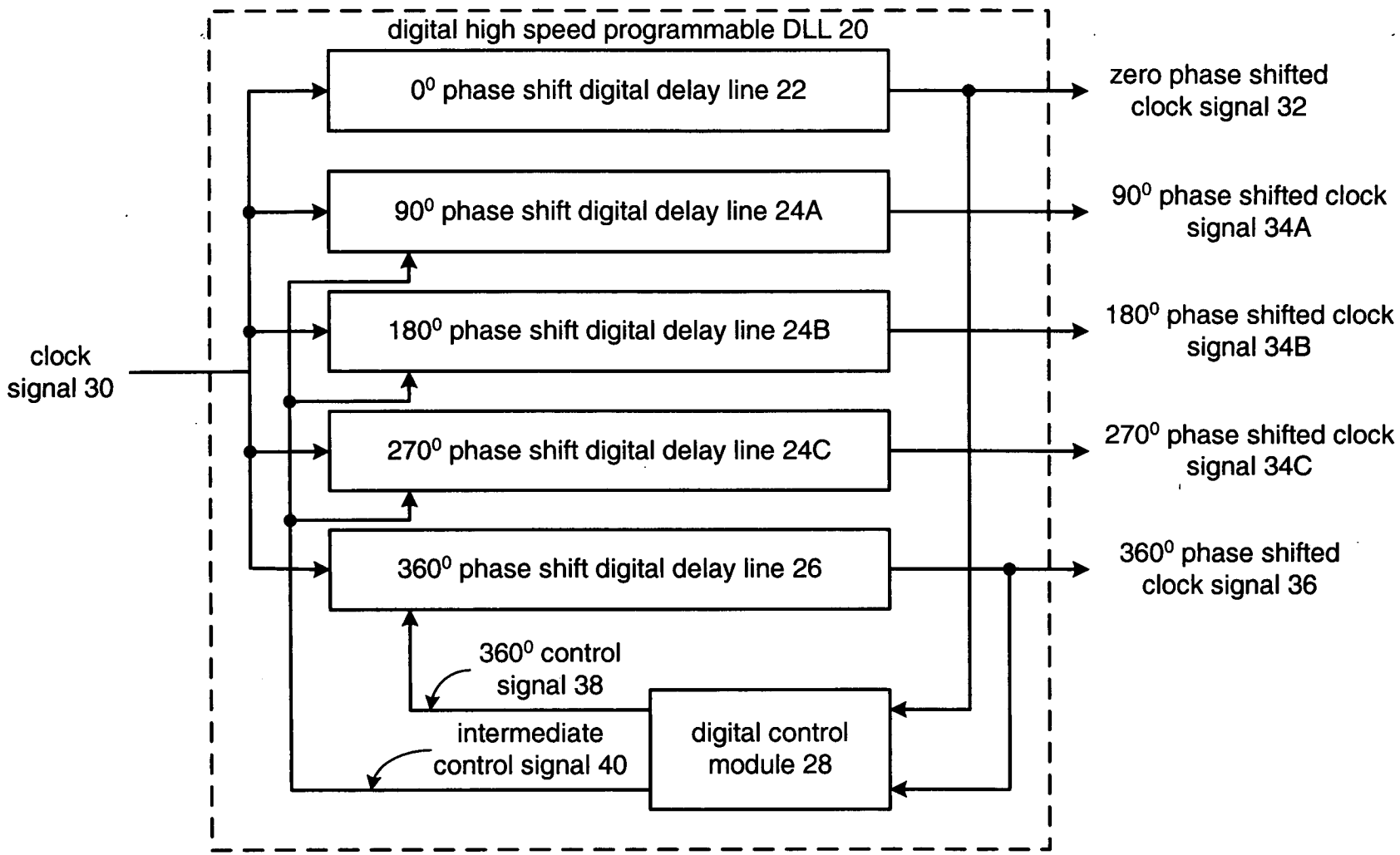

FIG. 3

digital clock manager

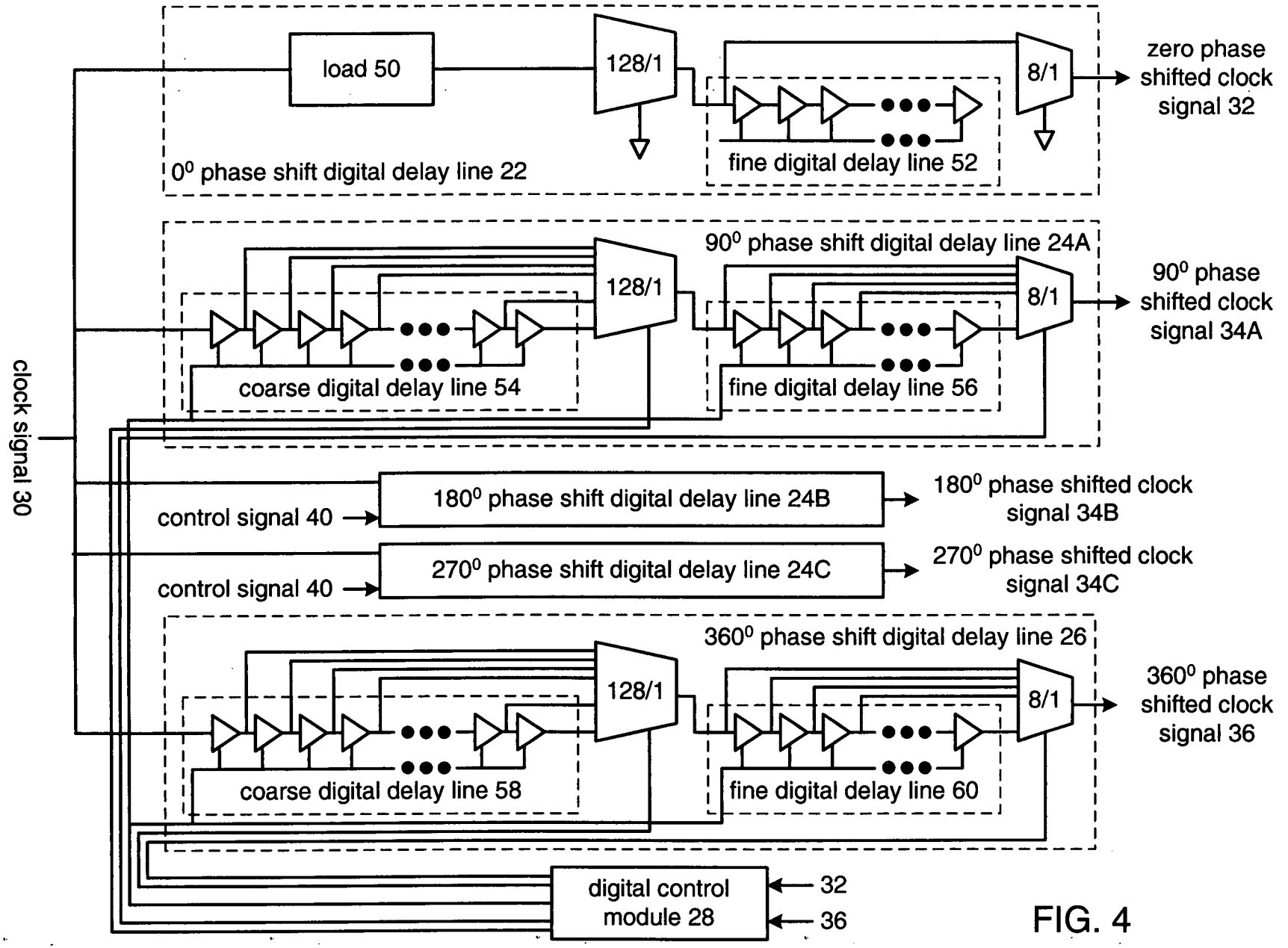
load 50
128/1
8/1
zero phase shifted clock signal 32
0⁰ phase shift digital delay line 22
fine digital delay line 52
90⁰ phase shift digital delay line 24A
128/1
8/1
90⁰ phase shifted clock signal 34A
coarse digital delay line 54
fine digital delay line 56
clock signal 30
control signal 40
180⁰ phase shift digital delay line 24B
180⁰ phase shifted clock signal 34B
control signal 40
270⁰ phase shift digital delay line 24C
270⁰ phase shifted clock signal 34C
360⁰ phase shift digital delay line 26
128/1
8/1
360⁰ phase shifted clock signal 36
coarse digital delay line 58
fine digital delay line 60
digital control module 28
32
36

FIG. 4

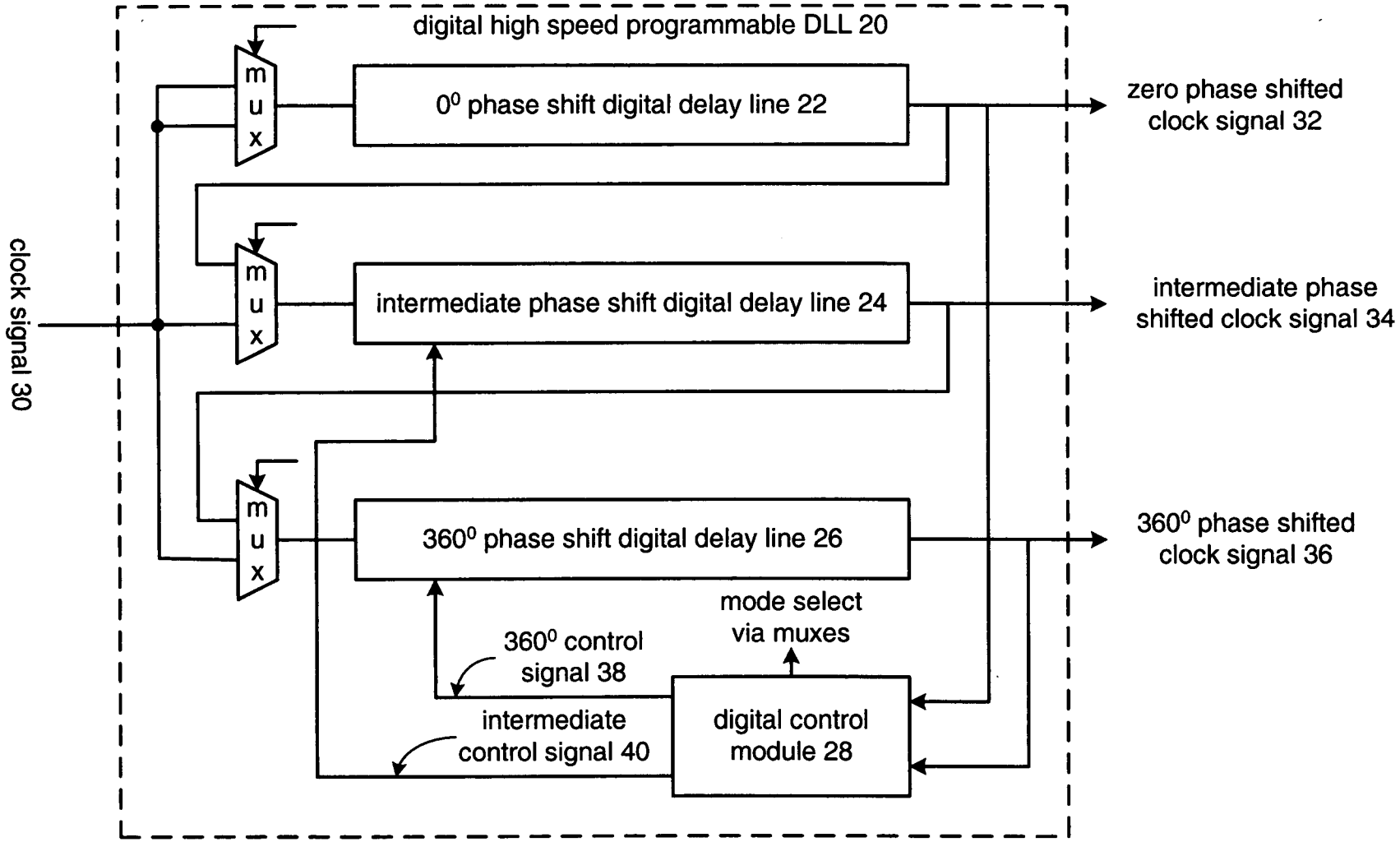

FIG. 5

digital clock manager